32733 (Pages : 3) Name.....

Reg. No.....

FIRST SEMESTER M.Sc. DEGREE (REGULAR/SUPPLEMENTARY) EXAMINATION, NOVEMBER 2022

(CBCSS)

Physics

PHY IC 04—ELECTRONICS

(2019 Admission onwards)

ne : Three Hours Maximum : 30 Weightage

Section A

Answer **all** *questions.*

Each question carries weightage 1.

1. What is unity-gain bandwidth of an operational amplifier ?
2. How can you change the frequency of emission in a LED ? Give any *two* examples for different colours.
3. Briefly explain radiative transition in a tunnel diode.
4. Write any *two* differences between common source and common drain operations of FET.
5. Briefly explain the advantages of Karnaugh map in logic circuit design.
6. Distinguish between microprocessor and Microcomputer.
7. Write a short note on population inversion.
8. How can you convert an SR Flip-flop to a JK Flip-flop ?

(8 × 1 = 8 weightage)

Section B

Answer any **two** *questions.*

Each question carries weightage 5.

9. With the help of a logic diagram explain the working of a ring counter.
10. How can you construct an active low pass filter using operational amplifier ? Explain its working.

Turn over

11. Explain the different biasing techniques used in JFET and also explain the working Source amplifier.

12. With the help of an R - 2R network circuit explain the conversion of a 4 bit digital sig signal.

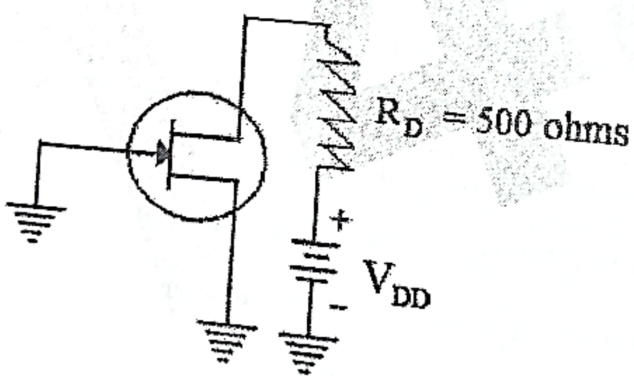
(2 × 5 = 1

Section C

Answer any **four** *questions.*
Each question carries weightage 3.

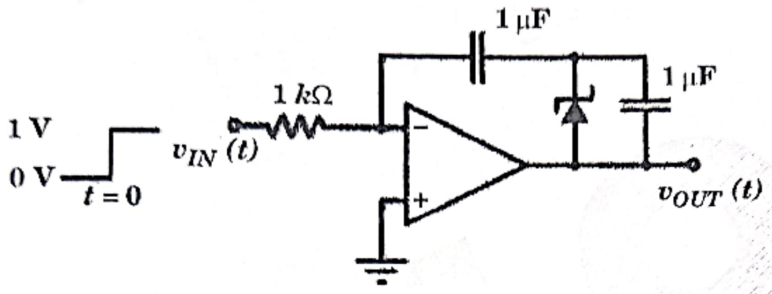
13. Show how an asynchronous counter can be implemented having a modulus of 12 wi binary sequence from 0000 through 1011.

14. For the JFET in the given figure, $V_{GS\ (off)}$ is – 3 V and I_{DSS} is 10 mA. Determine th value of V_{DD} required to put the device in constant current area of operation.



15. Design a practical differentiator that will differentiate signals with frequencies up to 40 gain at 10 Hz should be 0.12. If the op amp used in the design has a unity gain fre 2 MHz, what is the upper cutoff frequency of the differentiator ?

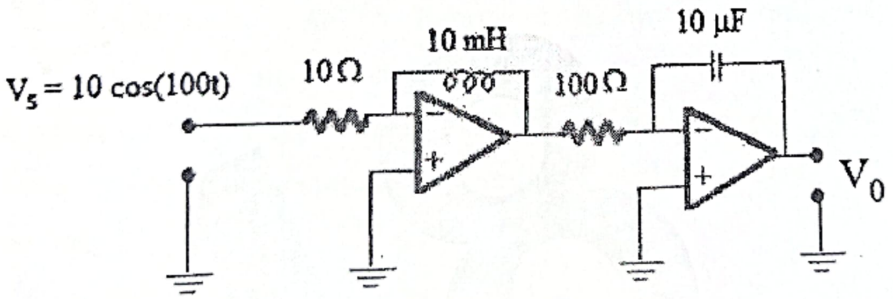
16. In the circuit shown below, the op-amp is ideal and Zener voltage of the diode is 2.5 volts. At the input, unit step voltage is applied, i.e. $v_{IN}(t) = u(t)$ volts. Also, at $t = 0$, the voltage across each of the capacitors is zero. Find the time 't' in milliseconds, at which the output voltage v_{OUT} crosses the Zener break down.



17. Using Karnaugh Map solve the given equation to reduce the number of gates used.

$Y - ABCD \mid \bar{A}BCD \mid AB\bar{C}D \mid AB\overline{CD}$.

18. In the figure given below assume the ideal op amp is used. Find the output voltage if an input signal Vs = 10 cos(100t) is applied.



. Draw the logical circuit of an synchronous decade counter.

(4 × 3 = 12 weightage)